REMARKS

Claims 1-24, 40-44 and 50-104 were pending up to this Amendment and Election.

Claims 56-58, 77, 90, 94, and 96 are rejected.

Claims 56-58, 77, 90, 94, and 96 are cancelled.

Claims 59, 78-79, 91-93, and 95 are objected to.

Claims 59, 78, 91, and 95 are amended.

Claims 1-24, 40-44, 50-55, 60-76, 80-89, and 97-104 are allowed.

Claims 1-24, 40-44, 50-55, 59-76, 78-89, 91-93, 95, and 97-104 are pending as a result of this Amendment.

Per the Examiner's objection to the title, Applicants have amended the title to "CIRCUIT AND METHOD FOR TIME-EFFICIENT MEMORY REPAIR." Per the Examiner's objection to the Abstract, Applicants are concurrently submitting a Replacement Abstract. Per the Examiner's rejection of claims 56-58, 77, 90, 94, and 96, Applicants are canceling those claims in favor of issuing the allowed claims. Applicants shall address the patentability of claims 56-58, 77, 90, 94, and 96 in a related application; hence, Applicants request the claims be cancelled without prejudice. Per the Examiner's objection to claims 59,78-79,91-93, and 95, Applicants have amended claims 59,78,91, and 95; as a result, the objected claims are now either independent or dependent upon an unrejected independent claim.

In light of the above amendments and remarks, Applicants submit that the pending claims are allowable. Therefore, Applicants respectfully request allowance of all of those claims. If there are any matters which may be resolved or clarified through a telephone interview, the Examiner is requested to contact Applicants' undersigned attorney at the number indicated.

Respectfully submitted,

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CORRECTED VERSION

~~Replacement~~ Abstract of the Disclosure

~~A preferred exemplary embodiment of the current invention concerns a memory testing process, wherein circuitry is provided to allow on-chip comparison of stored data and expected data. The on-chip comparison allows the tester to transmit in a parallel manner the expected data to a plurality of chips. In a preferred embodiment, at most one address -- and only the column address -- corresponding to a failed memory cell is stored in an on-chip address register at one time, with each earlier failed addresses being cleared from the register in favor of a subsequent failed address. Another bit -- the "fail flag" bit -- is stored in the address register to indicate that a failure has occurred. If the fail flag is present in a chip, that chip is repaired by electrically associating the column address with redundant memory cells rather than the original memory cells.~~Circuitry is provided to allow early switching of input signals from a first configuration directed to blow a first anti-fuse to a second configuration directed to blow a second anti-fuse, yet still allow complete blowing of the first anti-fuse. Such circuitry may be applied to methods of repairing a memory device after testing. Data concerning available ~~redundant~~repair cells may be stored in at least one on-chip redundancy register. ~~Additional circuitry is preferably provided to allow early switching of input signals from a first configuration directed to blow a first anti-fuse to a second configuration directed to blow a second anti-fuse, yet still allow complete blowing of the first anti-fuse. After repair, the chip's registers may be cleared and testing may continue. It is preferred that the address register and related logic circuitry be configured to avoid storing an address that is already associated with a redundant cell, even though that redundant cell has failed.~~